IN THE CLAIMS

1. (Previously Presented) A method of simulating a node using a simulation program that includes multiple, linked modules, the method comprising:

executing a first circuit module that simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit;

simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the acts of

forcing an initial forced logic state on the node;

after forcing, releasing the node from the initial forced logic state if a predetermined condition is met, which enables the simulation program to change a logic state of the node;

monitoring the node after the node has been released; and

providing an indication, in response to the monitoring, when the node is in a preselected condition.

2. (Previously Presented) The method of claim 1, wherein forcing the initial forced logic state includes forcing to a logic zero, logic one or high-impedance.

3. (Original) The method of claim 1, wherein releasing the node further comprises determining that the condition is met after passage of a predetermined amount of time.

4. (Previously Presented) The method of claim 3, wherein releasing the node further comprises determining that the condition is met when the node has been resolved.

5. (Previously Presented) The method of claim 1, wherein providing an indication includes indicating when the node is in an unknown logic state.

6. (Previously Presented) The method of claim 1, further comprising providing an error indication when the node is in a preselected condition.

7. (Original) The method of claim 3, further comprising selecting a user-defined time period for the predetermined amount of time.

8. (Previously Presented) A method of initializing and monitoring a simulated circuit node using a simulation program that includes multiple, linked modules, the method comprising:

executing a first circuit module that simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit;

simultaneously executing at least one behavior module, which is linked to the first circuit module, and which performs the acts of

obtaining an initial node condition for the node, wherein the initial node condition is a logic state;

forcing the node to the initial node condition;

after forcing, releasing the node from the initial node condition;

testing the node for a valid condition after the node has been released;

monitoring the node after the node has been released; and

providing an indication, in response to the monitoring, when the node is in an undesirable condition.

9. (Previously Presented) The method of claim 8, wherein the initial node condition is forced again if the testing indicates that the node has an unknown logic value.

10. (Previously Presented) The method of claim 9, wherein the initial node condition is forced and simulation is repeated until the node has a valid logic value.

11. (Previously Presented) The method of claim 10, wherein monitoring only occurs after the node has a valid logic value.

12. (Original) The method of claim 8, further comprising outputting the condition of the simulated node.

13. (Original) The method of claim 8, further comprising obtaining a simulation run time.

14. (Original) The method of claim 13, further comprising outputting a final node condition when the simulation run time is completed.

15. (Currently Amended) A computer-readable medium having computer-executable instructions comprising:

at least one selectable circuit module, which when executed simulates a circuit having a node, wherein the node represents a simulated electrical connection point of the circuit; and

at least one selectable behavior module, which is linkable to a circuit module, and which when executed simultaneously with the at least one selectable circuit module results in performing the following acts:

forcing an initial forced logic state on the node;

after forcing, releasing the node from the initial forced logic state if a predetermined condition is met, which enables a simulation program to change a logic state of the node;

monitoring the node after the node has been released; and

providing an indication, in response to the monitoring, when the node is in a preselected condition.

16. (Previously Presented) The medium of claim 15, having further computer-executable instructions for forcing the initial forced logic state to a logic zero, logic one or high-impedance.

17. (Original) The medium of claim 15, having further computer-executable instructions for determining that the condition is met after passage of a predetermined amount of time.

18. (Previously Presented) The medium of claim 15, having further computer-executable instructions for determining that the condition is met when the node has a valid logic value.

19. (Previously Presented) The medium of claim 18, having further computer-executable instructions for indicating when the node is in an unknown logic state.

20. (Currently Amended) A simulation module of a simulation program, the simulation module comprising:

an input means for inputting an initial node condition into a simulated circuit node of a circuit module linked with and simultaneously executable with the simulation module, wherein the simulated circuit node represents a simulated electrical connection point of the circuit module;

a conveying means for conveying the initial node condition to the simulated circuit node;

release means for releasing the simulated circuit node from the initial node condition upon satisfaction of a condition, wherein releasing the simulated circuit node occurs after conveying and enables the simulation program to change a logic state of the simulated circuit node;

a monitoring means for monitoring the simulated circuit node for a node condition after releasing the simulated circuit node from the initial node condition; and

an output means, responsive to the monitoring means, for outputting an indication when the node condition is in an undesirable state.

21. (Original) The module of claim 20, further comprising an output means for outputting the node condition.

22. (Original) The module of claim 20, further comprising an input means for inputting a simulation run time.

23. (Original) The module of claim 22, further comprising an output means for outputting a final node condition at completion of the simulation run time.

24. (Currently Amended) A computerized system for initializing and monitoring a simulated circuit node, the system comprising:

a circuit simulation tool;

at least one selectable circuit module, which when executed simulates a circuit having the simulated circuit node, wherein the simulated circuit node represents a simulated electrical connection point of the circuit; and

at least one selectable behavior module, which is linkable to and simultaneously executable with a circuit module, and which includes

a first input means for inputting an initial node condition;

a conveying means for conveying the initial node condition to the simulated circuit node;

a release means for releasing the initial node condition, wherein releasing the initial node condition occurs after conveying and enables the circuit simulation tool to change a logic state of the simulated circuit node;

a monitoring means for monitoring the simulated circuit node for a node condition after releasing the initial node condition;

a first output means for outputting an indication when the node condition is in an undesirable state, in response to the monitoring;

a second input means for inputting a simulation run time; and

a second output means for outputting a final node condition at completion of the simulation run time.

25. (Currently Amended) An HDL initial condition module comprising:

a means for maintaining a logic level of a simulated circuit node until a release condition is met, wherein

the simulated circuit node represents a simulated electrical connection point of a simulated circuit, and the simulated circuit is produced by an HDL circuit module that is linkable to the HDL initial condition module, and

a simulation program is able to change a logic state of the simulated circuit node after the release condition is met, wherein the release condition is when a known logic state can be determined for the simulated circuit node;

an initial condition release means, which enables the simulation program to change the logic level after the release condition is met; and

a simulated circuit node error detection means, which monitors the simulated circuit node for a node condition.

26-28. (Cancelled)

29. (Previously Presented) The module of claim 25, wherein the

means for maintaining the logic level of the simulated circuit node maintains the logic level for a predetermined period of time, and

wherein the module further comprises:

means for releasing an initial condition after the release condition is met, wherein the predetermined period of time is a simulation run time defined by an HDL simulation executable program.

30. (Original) The module of claim 29, wherein the predetermined period of time is a user-defined period of time.

31. (Previously Presented) An HDL simulated circuit device, comprising:

a circuit HDL module, which when executed simulates a circuit having a first simulated node, wherein the first simulated node represents a simulated electrical connection point of the circuit;

a first HDL module, linked to the circuit HDL module, the first HDL module including

a first input submodule inputting a first initial node condition,

a first conveyance submodule conveying the first initial node condition to the first simulated node,

a first monitor submodule monitoring the first simulated node for a first node condition, wherein monitoring occurs after conveying, and

a first output submodule outputting, in response to monitoring, a first indication when the first node condition is in an undesirable state;

a second HDL module, linked to the circuit HDL module, the second HDL module including

a second input submodule inputting a second initial node condition,

a second conveyance submodule conveying the second initial node condition to a second simulated node,

a release submodule releasing the second simulated node on a predetermined condition, wherein releasing the second simulated node enables a simulation program to change a logic level of the second simulated node,

a second monitor submodule monitoring the second simulated node for a second node condition, wherein monitoring occurs after releasing, and

a second output submodule outputting, in response to monitoring, a second indication when the second node condition is in an undesirable state; and

wherein the first conveyance submodule additionally conveys the first initial node condition to the second input submodule.

32. (Previously Presented) An HDL simulated circuit device, comprising:

a circuit HDL module, which when executed, simulates a circuit having a first simulated node, wherein the first simulated node represents a simulated electrical connection point of the circuit;

a first HDL module , linked to the circuit HDL module, the first HDL module including

a first input means for inputting a first initial node condition,

a first conveyance means for conveying the first initial node condition to the first simulated node, and

a first node condition output means for outputting a first indication when a first node condition is in an undesirable state, wherein outputting occurs after conveying;

a second HDL module, linked to the circuit HDL module, the second HDL module including

a second input means for inputting a second initial node condition, and

a second conveyance means for conveying the second initial node condition to a second simulated node; and

a third HDL module, linked to the circuit HDL module, the third HDL module including

a release condition means for releasing the second simulated node on a release condition, wherein releasing the second simulated node occurs after conveying and enables a simulation program to change a logic level of the second simulated node,

wherein the first node condition output means outputs the first node condition to the second input means if the release condition is valid.

33. (Currently Amended) An HDL design tool, comprising:

a circuit simulation device; and

a plurality of selectable modules capable of being linked to the circuit simulation device, wherein the plurality of selectable modules includes at least one selectable behavior module, which is linkable to a circuit module, and which when executed simultaneously results in

inputting an initial node condition into a simulated circuit node of the circuit module linked with the behavior module, wherein the simulated circuit node represents a simulated electrical connection point of the circuit module,

conveying the initial node condition to the simulated circuit node,

releasing the simulated circuit node from the initial node condition if a condition is met, wherein releasing the simulated circuit node occurs after conveying and enables the circuit simulation device to change a logic state of the simulated circuit node,

monitoring the simulated circuit node for a node condition, wherein monitoring occurs after releasing, and

outputting an indication, in response to monitoring, when the node condition is in an undesirable state.

34. (Currently Amended) A simulation method, comprising:

executing phase one by a behavior module, including

forcing an initial logic zero, logic one or high-impedance on a node of a circuit module linked with the behavior module, wherein the node represents a simulated electrical connection point of the circuit module,

releasing the node, wherein releasing the node enables a simulation program to change a logic state of the node, and wherein releasing occurs after forcing,

testing to see if the node has a valid logic value, wherein testing occurs after releasing,

if the node has the valid logic value, continuing to phase two, and

if the node does not have the valid logic value, continuing in phase one; and

simultaneously executing phase two by the behavior module, including

monitoring the node value,

testing the node value for a valid condition,

indicating an error if an unacceptable condition appears on the node, in response to monitoring and testing, and

continuing in phase two until simulation completion.

35. (Original) The method of claim 34, wherein simulation completion is a user defined time period.